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PATENT
Docket No. 18036-29

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application Of:

Lars G. Svensson, et al.

Serial Number: 09/758,631

Filing Date: January 10, 2001

Entitled: SYSTEM AND METHOD FOR POWER-EFFICIENT CHARGING AND DISCHARGING OF A CAPACITIVE LOAD FROM A SINGLE SOURCE

Group Art Unit:

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. § 1.56, the references listed on the attached Form PTO-1449 are being brought to the attention of the Examiner for consideration in connection with the examination of the above-captioned continuation reissue patent application. Copies of the cited documents are enclosed.

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made (37 C.F.R. § 1.97(g)), as an admission that the information cited is, or is considered to be, material to patentability, or that no other material information exists.

The filing of this Information Disclosure Statement shall not be construed as an admission against interest in any manner.

CONCLUDING REMARKS

It is respectfully requested that the examiner indicate consideration of the cited reference by returning a copy of the attached form PTO-1449 with initials or other appropriate marks with the first Office Action, and that the reference be made of record as a cited reference in the application.

Respectfully submitted,

Date: April 13, 2001

Marc E. Brown
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FORM PTO-1449 (Modified)	DOCKET NO. 18036-29	SERIAL NO. 09/758,631
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT: Svensson, Lars G., et al.	
	FILING DATE: January 10, 2001	Art Unit: Not known

UNITED STATES PATENT DOCUMENTS

*Exr's. Inits.	Ref.	Patent No.	Date	Name	Class	Sub Class	Filing Date (if applicable)
	AA	3,603,898	9/7/71	John Howard Dawson et al.	333	70	2/02/70
	AB	3,654,537	4/4/72	David W. Coffey	320	1	4/29/70
	AC	4,082,430	4/4/78	Peter U. Schulthess et al.	350	333	1/21/77
	AD	4,107,757	8/15/78	Senichi Masuda et al.	361	235	6/30/77
	AE	4,109,192	8/22/78	Ronald Brent Burbank et al.	320	1	6/25/76
	AF	4,328,525	5/04/82	Jay W. Allen et al.	361	152	6/27/80
	AG	4,594,589	6/10/86	Toshihiro Ohba et al.	340	805	8/27/82
	AH	4,605,999	8/12/86	Wayne C. Bowman et al.	363	19	3/11/85
	AI	4,707,692	11/17/87	Marvin L. Higgins et al.	340	805	11/30/84
	AJ	4,802,739	2/7/89	Yoshihiro Iwamoto	350	332	2/27/86
	AK	4,818,981	4/4/89	Ken-ichi Oki et al.	340	784	9/11/87
	AL	4,862,113	8/29/89	Otto R. Buhler et al.	331	117	1/06/88
	AM	4,893,117	1/9/90	Peter F. Blomley et al.	340	784	7/17/87

OTHER REFERENCES (Including Author, Date, Title, Pertinent Pages, Etc.)

Exr's. Inits.	Ref.	Bibliographic Data
	AN	Ammer, J., M. Bolotski, P. Alvelda, T.F. Knight, Jr., "TP12.5: A 160 x 120 Pixel Liquid-Crystal-on-Silicon Microdisplay with an Adiabatic DACM," In *1999 IEEE International Solid-States Circuits Conference Digest of Technical Papers*, pp. 212-213.
	AO	Ammer, J., M. Bolotski, P. Alvelda, T.F. Knight, Jr., "TP12.5: A 160 x 120 Pixel Liquid-Crystal-on-Silicon Microdisplay with an Adiabatic DAC," *1999 ISSCC Slide Supplement*, pp. 184-185, 435-.
	AP	Athas, William C., "Energy-Recovery CMOS," Chapter 5 in J. Rabaey, M. Pedram (Eds.) *Low-Power Design Methodologies*, Kluwer Academic Press, 1996.
	AQ	Athas, W.C. and L.J. Svensson, *Reversible Logic Issues in Adiabatic CMOS*, IEEE Workshop on Physics and Computation, 11/17-20/94 www.isi.edu/acmos
	AR	Athas, W.C., J. Koller and L. Svensson, *An Energy-Efficient CMOS Line Driver Using Adiabatic Switching,* University of Southern California, Information Sciences Institute Technical Report ACMOS-TR-2, 8/15/93, pp. 1-16.
	AS	Athas, W.C., J. Koller and L. Svensson, "An Energy-Efficient CMOS Line Driver Using Adiabatic Switching," *IEEE*, 1994, pp. 196-199.

Examiner	Date Considered

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	AT	4,920,474	4/24/90	Gert W. Bruning et al.	363	97	8/29/89
	AU	5,051,668	9/24/91	Seiji Kawaberi et al.	315	408	8/01/90
	AV	5,063,340	11/5/91	John A. Kalenowsky	320	1	10/25/90
	AW	5,095,223	3/10/92	Alexander C. Thomas	307	110	5/21/91
	AX	5,105,288	4/14/92	Koji Senda et al.	359	57	10/16/90
	AY	5,107,136	4/21/92	Michael A. W. Stekelenburg	307	269	3/29/90
	AZ	5,126,589	6/30/92	Herman L. Renger	307	270	8/31/90
	BA	5,150,013	9/22/92	Andrzej Bobel	315	209	5/6/91
	BB	5,206,632	4/27/93	Antoine Dupont et al.	340	784	9/11/90
	BC	5,247,376	9/21/93	Yoichi Wakai et al.	359	55	11/9/89
	BD	5,264,752	11/23/93	Joseph P. Savicki	310	316	6/1/92
	BE	5,293,082	3/8/94	Mehdi Bathaee	307	270	6/4/93
	BF	5,339,236	8/16/94	Akio Tamagawa	363	59	2/24/93

OTHER REFERENCES (Including Author, Date, Title, Pertinent Pages, Etc.)

Exr's. Inits.	Ref.	Bibliographic Data
	BG	Athas, W.C., L. "J." Svensson and N. Tzartzanis, "A Resonant Signal Drive For Two-Phase, Almost-Non-Overlapping Clocks," *IEEE International Symposium on Circuits and Systems*, May 1996.
	BH	Athas, W.C., N. Tzartzanis, L. Svensson, L. Peterson, H. Li, X. Jiang, P. Wang, W-C. Liu, "AC-1: A Clock-Powered Microprocessor," *IEEE Intl. Symposium on Low-Power Electronics and Design*, August 1997.
	BI	Athas, William C., Lars "J." Svensson, Jeffrey G. Koller, Nestoras Tzartzanis and Eric Ying-Chin Chou, "Low-Power Digital Systems Based on Adiabatic-Switching Principles," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 2, December 1994, pp. 398-407.
	BJ	Burr et al., "Energy Considerations in Multichip-Module Based Multiprocessors," *IEEE International Conference on Computer Design* 1991, pp. 593-600.
	BK	Chandrakasan et al., "Low-Power CMOS Digital Design," *IEEE Journal of Solid-State Circuits*, April 1992, Vol. 27, No. 4, pp. 473-484.

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*Exr's. Inits.	Ref.	Patent No.	Date	Name	Class	Sub Class	Filing Date (if applicable)
	BL	5,349,366	9/20/94	Shunpei Yamazaki et al.	345	92	10/27/92
	BM	5,459,414	10/17/95	Alexander G. Dickinson	326	93	5/28/93
	BN	5,465,054	11/07/95	Richard A. Erhart	326	34	4/8/94
	BO	5,473,269	12/5/95	Alexander G. Dickinson	326	93	11/4/94
	BP	5,473,526	12/5/95	Lars Svensson et al.	363	60	4/22/94
	BQ	5,506,520	4/09/96	David J. Frank et al.	326	96	1/11/95
	BR	5,508,639	4/16/96	John W. Fattaruso	326	97	1/13/95
	BS	5,510,748	4/23/96	Richard A. Erhart	327	530	1/18/94
	BT	5,517,145	5/14/96	David J. Frank	327	201	10/31/94
	BU	5,521,538	5/28/96	Alexander G. Dickinson	326	93	3/30/95
	BV	5,526,319	6/11/96	Robert H. Dennard et al.	365	226	1/31/95

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Exr's. Init.	Ref	Document No.	Date	Country	Class	Sub	Translation? Yes	No
	BW							
	BX							
	BY							

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Exr's. Inits.	Ref.	Bibliographic Data
	BZ	Davis, Andrew W. "Flat Panel Display Drivers: 'Little Things' Changing The Image Quality Picture," *Advanced Imaging*, October 1997, Vol. 12, No. 10, pp. 10, 12, 62.
	CA	Dharmasena, Sanjaya and Lars Svensson, "Startup Energies in Energy-Recovery CMOS," in Proceedings of Physics and Computation '96, Boston, MA, Nov 22-24, 1996.
	CB	Dickinson, Alex G. and John S. Denker, "Adiabatic Dynamic Logic," *IEEE, Custom Integrated Circuits Conference,* 1994, pp. 282-285.
	CC	Erhart, A. "P-10: Late Poster Paper: A High-Voltage High-Gray-Shade LCD Column Driver Utilizing a Standard 1.2-µm CMOS Process," *SID 94 Digest*, 1994, pp. 471-474.
	CD	Erhart, Alex. "Direct Drive Promises Reduced Power Consumption and Improved Image Quality for Notebook AMLCDs," *Information Display*, Dec. 1996, Vol. 12, No. 12, pp. 24-27.

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*Exr's. Inits.	Ref.	Patent No.	Date	Name	Class	Sub Class	Filing Date (if applicable)
	CE	5,528,256	6/18/96	Richard A. Erhart et al.	345	96	8/16/94
	CF	5,559,463	9/24/96	John S. Denker et al.	327	300	4/18/94
	CG	5,559,478	9/24/96	William C. Athas et al.	331	117	7/17/95
	CH	5,572,211	11/5/96	Richard A. Erhart et al.	341	144	1/18/94
	CI	5,578,957	11/26/96	Richard A. Erhart et al.	327	333	11/27/95
	CJ	5,602,497	2/11/97	Steven D. Thomas	326	93	12/20/95
	CK	5,604,449	2/18/97	Richard A. Erhart et al.	326	81	1/29/96
	CL	5,604,454	2/18/97	Jeffrey E. Maguire et al.	327	112	9/29/95
	CM	5,657,039	8/12/97	Katsuya Mizukata et al.	345	95	11/3/94
	CN	5,675,263	10/07/97	Thaddeus J. Gabara	326	97	11/21/95
	CO	5,694,445	12/02/97	Hiroshige Hirano et al.	377	57	9/20/95

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Exr's. Init.	Ref	Document No.	Date	Country	Class	Sub	Translation? Yes	No
	CP							

OTHER REFERENCES (Including Author, Date, Title, Pertinent Pages, Etc.)

Exr's. Inits.	Ref.	Bibliographic Data
	CQ	*Flat Panel Display Handbook, Technology Trends & Fundamentals*, First Edition, 1999, San Jose: Stanford Resources, 1999.
	CR	Fundaun, I., C. Reese and H.H. Soonpaa (Physics Department, University of North Dakota, Grand Forks), "Charging a capacitor," *American Journal of Physics*, Volume 60, No. 11, Nov. 1999, pp. 1047-1048.
	CS	Heinrich, F. (Laboratory of Solid State Physics, Swiss Federal institute of technology ETH), "Entropy Change When Charging A Capacitor: A Demonstration Experiment, *American Journal of Physics*, Vol. 54, No. 8, August 1986, pp. 742-744.
	CT	Jonscher, A.K. (Royal Holloway and Bedford New College, Univ. of London), "Charging and Discharging of Non-Ideal Capacitors," *IEEE Transactions on Electrical Insulation*, Vol. EI-22, No. 4, August 1987, pp. 357-359.
	CU	Kawahara, T., M. Horiguchi, Y. Kawajiri, T. Akiba, G. Kitsukawa, T. Kure, and M. Aoki. "A Charge Recycle Refresh for Gb-scale DRAMs in File Applications," *1993 Symposium on VLSI Circuits, Digest of Technical Papers*, May 19-21, 1993, pp. 41-42.

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*Exr's. Inits.	Ref.	Patent No.	Date	Name	Class	Sub Class	Filing Date (if applicable)
	CV	5,734,285	3/31/98	Geoffrey P. Harvey	327	291	12/17/93
	CW	5,748,165	5/5/98	Yashushi Kubota et al.	345	96	12/23/94
	CX	5,754,156	5/19/98	Richard Alexander Erhart et al.	345	98	9/19/96
	CY	5,818,252	10/6/98	Edward Carl Fullman et al.	324	765	9/19/96
	CZ	5,821,923	10/13/98	Alfonsus M. Van Amesfoort et al.	345	212	2/23/96
	DA	5,838,203	11/17/98	Georgios Stamoulis et al.	331	1 A	12/6/96
	DB	5,838,289	11/17/98	Hideki Saito et al.	345	79	9/26/95
	DC	5,841,299	11/24/98	Vivek K. De	326	98	2/6/97
	DD	5,852,426	12/22/98	Richard Alexander Erhart et al.	345	96	3/21/96
	DE	5,861,861	1/19/99	James B. Nolan et al.	345	87	6/28/96
	DF						

FOREIGN PATENT DOCUMENTS

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	DG							
	DH							
	DI							

OTHER REFERENCES (Including Author, Date, Title, Pertinent Pages, Etc.)

Exr's. Inits.	Ref.	Bibliographic Data
	DJ	Koller, Jeffrey G. and William C. Athas, "Adiabatic Switching, Low Energy Computing, and the Physics of Storing and Erasing Information," IEEE Press 1993, pp. 267-270.
	DK	Lieberman, David, "EL Design Yields Brighter Display At Lower Power," *Electronic Engineering Times*, No. 1021, August 1998, pp. 52-.
	DL	Maksimovic, Dragan, "A MOS Gate Drive With Resonant Transitions," IEEE Press, 1991, pp. 527-532.
	DM	Mateo, D. and A. Rubio, "Quasi-adiabatic ternary CMOS logic," *Electronics Letters*, Vol. 32, No. 2, 1/18/96, pp. 99-101.
	DN	Mead et al., "Chapter 1, MOS Devices and Circuits," In *Introduction to VLSI Systems*, 1980, Addison-Wesley, pp. 1-37.

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	DO	5,870,331	2/09/99	Yi-Ren Warry Hwang et al.	365	154	9/26/97
	DP	5,880,602	3/9/99	Yasuo Kaminaga et al.	326	81	2/28/96
	DQ	5,881,014	3/9/99	Tsukasa Ooishi	365	226	8/19/97
	DR	5,883,538	3/16/99	Brent Keeth et al.	327	333	5/21/97
	DS	5,889,439	3/30/99	Robert Meyer et al.	331	17	8/20/97
	DT	5,892,540	4/6/99	Lester J. Kozlowski et al.	348	300	6/13/96
	DU	5,896,117	4/20/99	Seung-Hawn Moon	345	95	6/27/96
	DV	5,900,854	5/4/99	Hiroji Itoh et al.	345	99	9/28/95
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	DZ							
	EA							

OTHER REFERENCES (Including Author, Date, Title, Pertinent Pages, Etc.)

Exr's. Inits.	Ref.	Bibliographic Data
	EB	Morimura, Hiroki and Nobutaro Shibata, "A 1-V 1-Mb SRAM for Portable Equipment," *ISLPED, 1996 Monterey CA USA*, pp. 61-66.
	EC	Nordin et al., "A Systems Perspective on Digital Interconnection Technology," *IEEE Journal of Lightwave Technology*, June 1992, Vol. 10, no. 6, pp. 811-827.
	ED	*RCA Transistor Thyristor & Diode Manual*, RCA Corporation, 4/71, Technical Series SC-15, 1971, pp. 179-183.
	EE	Schlig, E.S. and J.L. Sanford. "New Circuits for AMLCD Data Line Drivers," 1994.
	EF	Seitz et al., "Hot-Clock nMOS," *Proceedings of the 1985 Chapel Hill Conference on VLSI*, 1985, pp. 1-17

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	ER							
	ES							

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Exr's. Inits.	Ref.	Bibliographic Data
	ET	Sekiguchi, Tomonori, Masashi Horiguchi, Takeshi Sakata, Yoshinobu Nakagome, Shigeki Ueda and Masakazu Aoki, "Low-Noise, High-Speed Data Transmission Using a Ringing-Canceling Output Buffer," *IEEE Journal of Solid-State Circuits*, Vol. 30, No. 12, 1995, pp. 1569-1574.
	EU	Somasekhar, Dinesh, Yibin Ye and Kaushik Roy. "An Energy Recovery Static RAM Memory Core," in *IEEE Symposium on Low-Power Electronics*, 2d ed., 1995, pp. 62-63.
	EV	Svensson L. et al., *Adiabatic Charging Without Inductors*, USC/ISI Technical Report ACMOS-TR-3, December 17, 1993.
	EW	[Svensson, L.J.] LS. "LCD Driver Test Chip Evaluation," October 21, 1996.
	EX	Svensson, L. "J.", W.C. Athas and R.S.-C. Wen, "A sub-CV^2 pad driver with 10 ns transition time," *ISLPED 1996 Monterey CA USA*, 8/96, pp. 105-108.

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	FH						
	FI						
	FJ						

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Exr's. Inits.	Ref.	Bibliographic Data
	FK	Svensson, L. "J." and W.C. Athas, "Stepwise Charging Without Equations," USC/ISI, 2/25/97, pp. 1-4.
	FL	Tzartzanis, Nestor and William C. Athas, "Clock-Powered CMOS: A Hybrid Adiabatic Logic Style for Energy-Efficient Computing," *20th Anniversary Conference on Advanced Research in VLSI*, IEEE Computer Society Press, March 1999.
	FM	Tzartzanis, Nestor and William C. Athas, "Energy Recovery for the Design of High-Speed, Low-Power Static RAMs," *International Symposium on Low-Power Electronics and Design,* August 1996. *Monterey CA USA,* pp. 55-60.
	FN	Tzartzanis, Nestor, *Energy-Recovery Techniques for CMOS Microprocessor Design*, Ph.D. Dissertation, University of Southern California, August 1998, 163 pp.
	FO	Weste et al., "Principles of CMOS VLSI Design, A Systems Perspective," Chapter 5 in *CMOS Circuit and Logic Design*, 2d Edition, 1993, Addison-Wesley, pp. 160-231. [need copy of document.]
	FP	Ye, Yibin and Roy Kaushik, "Energy Recovery Circuits Using Reversible and Partially Reversible Logic," *IEEE Transactions on Circuits and Systems – I. Fundamental Theory,* Vol. 43, No. 9, 1996, pp. 769-778.

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	FX						
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Exr's. Inits.	Ref.	Bibliographic Data
	GA	Younis, Saed G. and Thomas F. Knight, Jr., "Non-Dissipative Rail Drivers for Adiabatic Circuits," *IEEE*, 9/95, pp. 404-414.
	GB	Yuan, Jiren (Linkoping University), "Low Power and Low Area or High Throughput Single-Ended Bus and I/O Protocols," *Proceedings of 1997 IEEE International Symposium on Circuits and Systems: Circuits and Systems in the InformationAge, ISCAS '97, June 9-12, 1997, Hong Kong*, pp. 1932-1935.
	GC	
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